

Compact Monolithic Integrated Resistive Mixers With Low Distortion for HIPERLAN

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Abstract—Three ultra-compact low-cost mixers, using either a single enhancement, depletion, or deep-depletion FET are presented and compared in this paper. They are designed for HIPERLAN and 802.11a receivers with radio and intermediate frequencies around 5.2 and 0.95 GHz, respectively. An improved MESFET large-signal model has been used to allow efficient optimizations of the circuits. The fully integrated mixers have been fabricated using a commercial 0.6- μm GaAs MESFET process and require a total chip area of only 0.5 mm². With an ultra-low local-oscillator (LO) power of -10 dBm, the enhancement FET mixer achieves a -4.7 dBm 1-dB input compression point, a 12.6-dB conversion loss, and a 13-dB noise figure. At a low LO power of -2.5 dBm, excellent dynamic properties are obtained for the depletion FET mixer with 2.6-dBm 1-dB input compression point, 8.3-dB conversion loss, and 8.8-dB noise figure. State-of-the-art performances with 16-dBm 1-dB input compression point, 5.5-dB conversion loss, and 6.5-dB noise figure are reached for the deep depletion FET mixer at 10-dBm LO power.

Index Terms—MESFET, MMIC mixers, passive circuits, wireless LAN.

I. INTRODUCTION

IN RECENT years, demands for mixers in wireless systems are continuously increasing in terms of conversion loss (gain), noise figure, and dynamic range. Furthermore, circuit size and required local-oscillator (LO) power have to be minimized, to keep pace with the advancing improvements, concerning miniaturization and power consumption. Much work about mixers has been published, using either active or passive topologies [1], [2]. With the upcoming trend to decrease supply voltages of receivers down to the voltage of one single battery cell ($V_{\text{supply}} \leq 1.2$ V), it is becoming more and more difficult for active mixers to meet the requirements for linearity and intermodulation. However, passive mixers have the significant advantage of not being dependent on any supply voltage. Promising approaches have been reported, using passive FETs [3]–[6] as the mixing elements. Mixing is enabled by varying the channel resistance of the transistors. Due to the weak nonlinearity of this resistance, those resistive mixers allow excellent intermodulation performances.

In this paper, we propose ultra-compact fully integrated resistive mixers for application in HIPERLAN (Europe) and 802.11a transceivers (U.S.) at *C*-band. The circuits have been fabricated using a commercial 0.6- μm GaAs process (Triquint TQTRx) to enable mass fabrication. This foundry process

features enhancement (E), depletion (D), and depletion power (G) FETs. The performances and the corresponding tradeoffs of three mixers using these different transistors are discussed and compared. State-of-the-art performances in terms of conversion loss, noise figure, and large-signal behavior are reached. The simple topology of the mixer monolithic microwave integrated circuits (MMICs) enables high yield. An overall chip area of only 0.5 mm² each is required. This makes the mixers very well suited for low-cost applications.

II. DESIGN

Small- and large-signal optimizations have been performed in a harmonic-balance simulator in HP CDS, applying our MESFET large-signal model [7], which allows excellent predictions in the resistive region of MESFETs.

The circuit topology of the three mixers, using either a single E-, D- or G-FET, is shown in Fig. 1, with element values specified for the D-FET mixer. Due to the similarity of the different FETs in terms of matching, the circuit topology can be applied for all three mixers by slightly adapting the capacitor and inductor values. Matching for the LO, IF, and RF port to 50 Ω is achieved by using *LC* filters. A further task of these filters is to suppress undesired frequency components in order to improve port-to-port isolations and to decrease noise and conversion loss. Linewidths and spacings of 5 μm have been used for the inductors. Line thicknesses are 4 μm . Quality factors (Q) of approximately 20 at 5 GHz and 9 at 1 GHz have been measured for these inductors.

FETs with gatewidths of 500 μm have been chosen to fulfill a good tradeoff between ease of matching and conversion efficiency on one hand (large gatewidths required), and port to port isolation and LO power requirements on the other hand (small gatewidths required). The gate lengths of 0.6 μm , the gate-to-source distances of 0.6 μm , and the gate-to-drain distances of 1 μm are defined by the foundry process. The *I/V* characteristics of these FETs in their resistive region are shown in Fig. 2. From the *I/V* characteristics, resistances from an open circuit down to 5, 7, and 13 Ω can be estimated for the G-, D- and E-FET mixers, respectively. These ranges are suited to realize resistive mixers with good conversion efficiencies. The best conversion efficiency can be forecasted for the G-FET mixer, having the lowest channel resistance at high LO power.

The FET gate bias voltages, optimized to obtain minimum conversion losses, are $V_{\text{dc},\text{E-FET}} = 0.2$ V, $V_{\text{dc},\text{D-FET}} = -0.5$ V, and $V_{\text{dc},\text{G-FET}} = -1.5$ V. These voltages are near the corresponding pinchoff voltages ($V_{\text{th},\text{E-FET}} = 0.15$ V, $V_{\text{th},\text{D-FET}} = -0.6$ V, and

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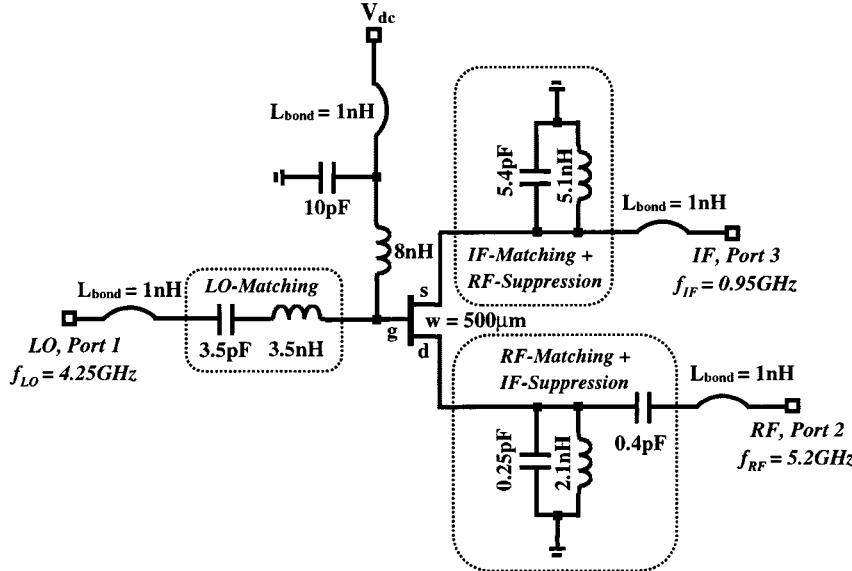


Fig. 1. Circuit topology of the resistive mixers, element values are for the mixer using the depletion type (D) MESFET, LO: local oscillator, IF: intermediate frequency, RF: radio frequency.

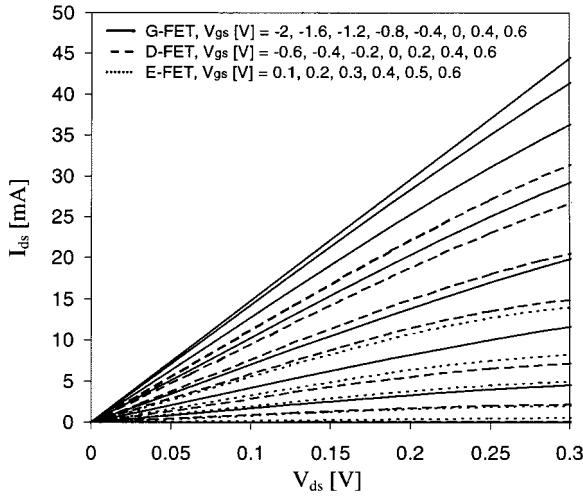


Fig. 2. I/V characteristics of the enhancement (E), depletion (D), and depletion power (G) FET with gatewidths of $300\ \mu\text{m}$.

$V_{\text{th},\text{G-FET}} = -2\ \text{V}$), around which high variations of the channel resistance are achieved. In comparison to the D-FET and G-FET mixers, the E-FET mixer has the advantage of having a positive bias voltage. The gate bias voltages are fed through RF chokes with high- Q , in order to minimize self-biasing effects. Simulations showed that those self-biasing effects significantly decrease the performance of the mixers, especially when applying high LO power. If the inductor had high ohmic series resistance, a voltage drop along the resistance would be created by the LO power, therefore changing the bias and degrading the performances of the mixers. The drain and source of the FETs are dc grounded by the inductors of the RF and IF filter, respectively.

A photograph of the mixer MMIC using the G-FET is shown in Fig. 3. Each of the three mixers has an overall chip size of $0.9\ \text{mm} \times 0.6\ \text{mm}$.

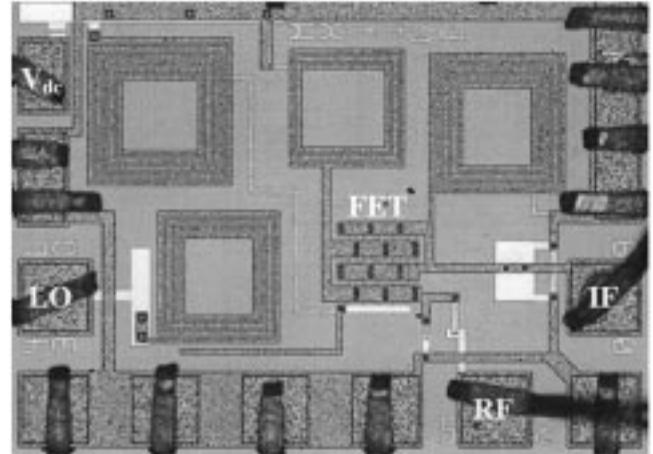


Fig. 3. G-FET mixer MMIC (overall chip size is $0.9\ \text{mm} \times 0.6\ \text{mm}$).

III. RESULTS

For measurements, the circuits were mounted and bonded on a $1'' \times 1''$ Duroid test substrate. This substrate causes moderate path losses of around $0.15\ \text{dB}$ at $5\ \text{GHz}$ and less than $0.1\ \text{dB}$ at $1\ \text{GHz}$. S -parameters have been measured with an HP 8510B network analyzer. Large-signal performances have been measured with Marconi 2042 signal generators and an HP 8565E spectrum analyzer. Noise has been measured with an HP 8970B/8971C noise-figure test set.

Fig. 4 illustrates the conversion loss versus applied LO power for the three mixers. Receivers with ultra-low-power consumption are able to provide only a very low LO power. The E-FET mixer is the first choice for such systems because moderate variations of the channel resistance of the E-FET are achieved with minimum LO power. At an ultra-low LO power of only $-10\ \text{dBm}$, a conversion loss of $12.6\ \text{dB}$ was measured. This conversion loss is relatively high. However, the reduced dc power consumption allows to add a low-noise RF amplifier in front of the mixer or an IF amplifier behind the mixer. For a compact

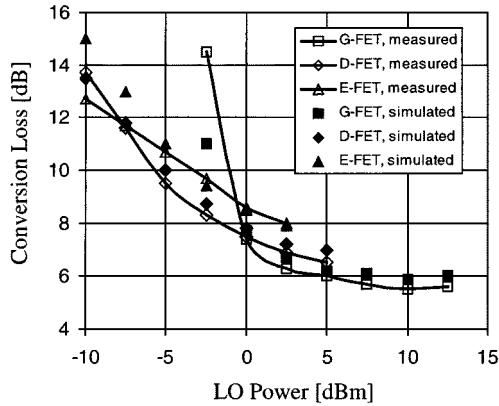


Fig. 4. Measured conversion loss versus applied LO power for the mixers using the E-, D- or G-FET.

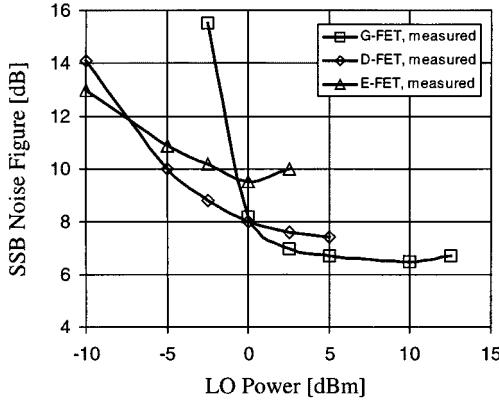


Fig. 5. Measured SSB noise figure versus applied LO power for the mixers using the E-, D- or G-FET.

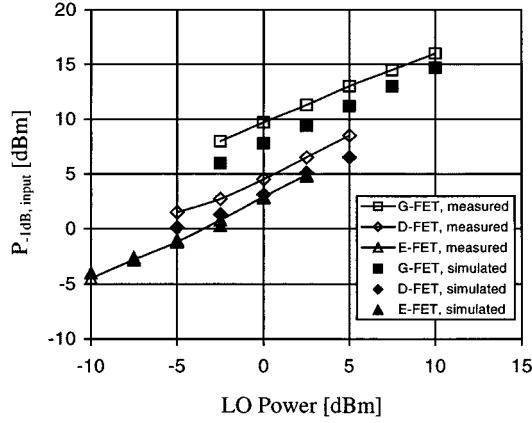


Fig. 6. Measured 1-dB input compression point versus applied LO power for the mixers using the E-, D-, or G-FET.

ultra-low power-consuming *C*-band low-noise amplifier with a gain/dc power-consumption figure-of-merit of $S_{21}/P_{dc} = 10$ dB/mW, it is referred to [8].

The D-FET mixer is well suited for a low LO power from -5 to 0 dBm. At an LO power of -2.5 dBm, a conversion loss of 8.3 dB was measured.

The G-FET mixer can be driven with high LO power, thus allowing high variations of the channel resistance of the FET and thereby enabling low conversion loss. At an LO power of

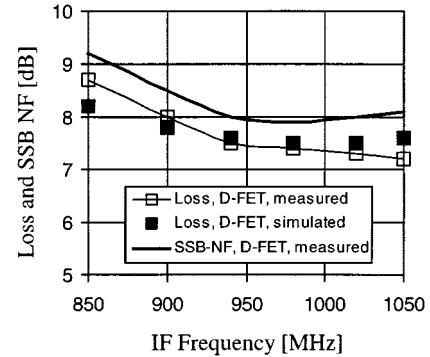


Fig. 7. Measured conversion loss and SSB noise figure versus frequency of the D-FET mixer, $P_{LO} = 0$ dBm, RF frequency is swept from 5.1 to 5.3 GHz, $f_{LO} = 4.25$ GHz.

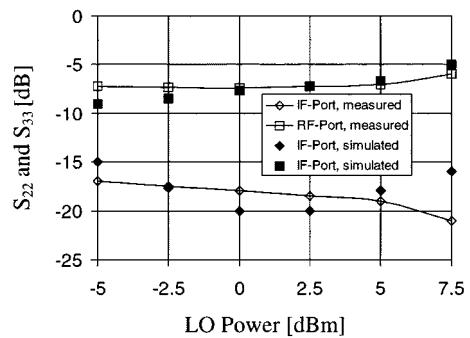


Fig. 8. Measured return losses versus LO power of the D-FET mixer.

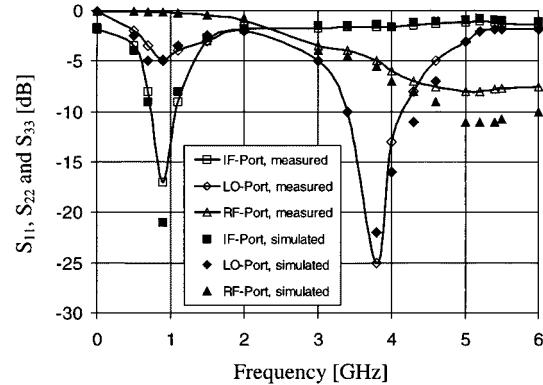


Fig. 9. Measured return losses versus frequency of the D-FET mixer at an LO power of -2.5 dBm.

10 dBm, a very low conversion loss of only 5.5 dB was measured.

In Fig. 5, the single-sideband (SSB) noise figure versus the applied LO power (P_{LO}) is shown. Noise figures of $NF_{G\text{-FET}} = 6.5$ dB ($P_{LO} = 10$ dBm), $NF_{D\text{-FET}} = 8.8$ dB ($P_{LO} = -2.5$ dBm), and $NF_{E\text{-FET}} = 13$ dB ($P_{LO} = -10$ dBm) are measured.

Fig. 6 illustrates the 1-dB input compression point versus LO power. Excellent 1-dB input compression points of $P_{1\text{dB,E-FET}} = -4.7$ dBm ($P_{LO} = -10$ dBm), $P_{1\text{dB,D-FET}} = 2.6$ dBm ($P_{LO} = -2.5$ dBm), and $P_{1\text{dB,G-FET}} = 16$ dBm ($P_{LO} = 10$ dBm) are measured for the passive mixers. Active mixers would require a very high dc power to reach comparable performances.

TABLE I
PORT-TO-PORT ISOLATIONS OF THE D-FET MIXER AT 0-dB LO AND RF POWER

Isolation	LO to IF	LO to RF	RF to IF	RF to LO	IF to RF	IF to LO
Simulations	15dB	11dB	22dB	15dB	35dB	33dB
Measurements	17dB	14dB	22dB	19dB	30dB	29dB

TABLE II
RESISTIVE MIXER COMPARISON

Technology	MMIC					HMIC	
	E-FET	D-FET	G-FET	E-FET	HEMT	D-FET	D-FET
GaAs transistor							
Gate length		0.6 μ m		0.6 μ m	0.13 μ m	n.a.	0.8 μ m
RF/IF		5.2GHz/ 0.95GHz		1.9GHz/ 110MHz	25.7GHz/ 200MHz	10.5GHz/ 1.5GHz	2.6GHz/ 300MHz
LO power	-10dBm	0dBm	10dBm	-5dBm	10dBm	10dBm	8dBm
Conversion loss	12.6dB	7.4dB	5.5dB	7dB	7.2dB	6.5dB	9dB
SSB-NF	13dB	7.9dB	6.5dB	8dB	n.a.	6.6dB	9.2dB
P _{1dB, In}	-4.7dBm	4dBm	16dBm	-1.5dBm	7dBm	16.5dBm	12dBm
IIP3	2dBm	13dBm	23dBm	8dBm	n.a.	27dBm	18dBm
Bias	positive	negative	negative	0V	negative	negative	negative
Circuit area	0.5mm ²			0.7mm ²	4.5mm ²	Large (hybrid), exact area n.a.	
Reference	This work			[5]	[6]	[3]	[4]

[9]. The measured third-order intercept points at the input are $IIP3_{E-FET} = 2$ dBm ($P_{LO} = -10$ dBm), $IIP3_{D-FET} = 11.5$ dBm ($P_{LO} = -2.5$ dBm), and $IIP3_{G-FET} = 23$ dBm ($P_{LO} = 10$ dBm).

In the following, the focus is put on the D-FET mixer. However, the results obtained for the G- and E-FET mixers are similar.

In Fig. 7, the conversion loss and the SSB noise figure of the D-FET mixer is plotted versus IF frequency at an LO power of 0 dBm. With the RF frequency swept from 5.15 to 5.3 GHz, and a constant LO frequency of 4.25 GHz, the conversion loss and the noise figure are less than 8 and 8.4 dB, respectively, making the mixer well suited for HIPERLAN and 802.11a receivers.

The RF and IF return losses versus LO power of the D-FET mixer are illustrated in Fig. 8. Within an LO power range from -5 up to 5 dBm, the return losses are higher than 6.5 dB for the RF port and 16.5 dB for the IF port. The return losses versus frequency of the D-FET mixer at an LO power of -2.5 dBm are plotted in Fig. 9. They are 8, 8.3, and 13.2 dB for the RF, LO, and IF port, respectively. The return losses are not very high because the circuits were optimized for minimum conversion losses and not for maximum return losses. The measured port-to-port isolations of the D-FET mixer are listed in Table I. They are between 14–30 dB.

Good agreement between all measurements and simulations have been obtained, thereby verifying the accuracy of our MESFET large-signal model.

In Table II, the designed mixers are compared with state-of-the-art resistive mixers using MMIC or hybrid microwave integrated circuit (HMIC) technology. To the knowledge of the authors, the conversion loss and noise figure of the designed G-FET mixer are the lowest for resistive mixers reported to date. These results can successfully compete with state-of-the-art single-diode mixers [3, Table I]. However, the presented G-FET mixer has significantly better large-signal properties and an ultra-compact size.

IV. CONCLUSIONS

The design and the results of three resistive mixer MMICs for HIPERLAN and the 802.11a standard at C -band have been presented using either a single E-, D-, or G-FET. An improved MESFET large —signal model has been used to allow efficient optimizations of the circuits. Excellent linearity performances have been reached for these mixers at ultra-low as well as for high LO levels, thereby enabling various applications. Due to their compact sizes and the utilization of a commercial GaAs process, the circuits are well suited for low-cost mass fabrication. To the knowledge of the authors, the results for the G-FET mixer, concerning conversion loss and noise figure, are the best for resistive mixers with one single transistor reported to date.

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